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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/071,014	02/07/2002	Peter L. Fu	005858P7148	8752

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EXAMINER	
MCLEAN MAYO, KIMBERLY N	

ART UNIT	PAPER NUMBER
2187	2

DATE MAILED: 06/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/071,014	FU, PETER L.	
	Examiner	Art Unit	
	Kimberly N. McLean-Mayo	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8,12-14 and 17-24* is/are rejected.

7)☒ Claim(s) *6,7,9-11,15 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The enclosed detailed action is in response to the Application submitted on February 7, 2002.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Skazinski et al. (USPN: 6,574,709).

Regarding claim 1, Skazinski discloses a method for maintaining dirty data comprising receiving a request to write data to a memory location that is cached to a cache (Figure 7, Reference 305; C 18, L 61-64); writing data to a plurality of cache lines in the cache, the plurality of cache lines written to being duplicate cache lines (Figure 7, Reference 340; C 19, L 42-44); and marking the duplicate cache lines dirty (C 22, L 50-53; each controller contains a CLD which includes a dirty block mirror map [C 3, L 60-67; C 4, L 1-2; C 9, L 59-67; C 10, entire; and specifically, C 11, L 23-34]). Additionally, with respect to claim 12, all hardware systems include computer readable mediums [memory] storing instructions [code] to execute operations [such as the above functions] of the system.

4. Claims 1, 3-5, 8 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Loechel (USPN: 5,895,485).

Regarding claim 1, Loechel discloses a method for maintaining dirty data comprising receiving a request to write data to a memory location that is cached to a cache (C 3, L 55-56); writing data to a plurality of cache lines in the cache, the plurality of cache lines written to being duplicate cache lines (C 3, L 56-58); and marking the duplicate cache lines dirty (C 8, L 2-9; each cache line contains a dirty map which is set whenever data at the corresponding cache line has been written but has not been written to the main storage). Additionally, with respect to claim 12, all hardware systems include computer readable mediums [memory] storing instructions [code] to execute operations [such as the above functions] of the system.

Regarding claims 3 and 14, Loechel discloses reading data from a first dirty cache line in a plurality of cache lines in a cache, the first dirty cache line corresponding to a first memory location (Figure 10, Reference 1004; when the cache lines are flushed, the lines are read out of the cache and then written to the persistent storage); determining if the data is corrupt (C 1, L 8-10; C 4, L 41-42; this is determined by the occurrence or non-occurrence of a cache failure of a first cache during a cache flush operation); if the data is not corrupt [if no failure has occurred] then writing [flushing] the data to the first memory location (C 9, L 26-27); marking the cache line available [clearing the dirty bit] (when the cache lines are written are to the persistent memory, the lines are cleared in the cache); determining at least one duplicate dirty cache line of the first dirty cache line and marking each of the at least one duplicate dirty cache line as an

available cache line (Figure 10, Reference 1006). Additionally, with respect to claim 14, all hardware systems include computer readable mediums [memory] storing instructions [code] to execute operations [such as the above functions] of the system.

Regarding claims 4-5, Loechel discloses marking the duplicate dirty cache lines invalid (C 7, L 63-65; when the data contains invalid data the cache lines are marked invalid).

Regarding claim 8, Loechel discloses reading data from a first dirty cache line in a plurality of cache lines in a cache, the first dirty cache line corresponding to a first memory location (Figure 10, Reference 1004; when the cache lines are flushed, the lines are read out of the cache and then written to the persistent storage); determining if the first cache line is a clean line (inherently the systems determines this by determining that the line is dirty and needs to be flushed which also indicates that the line is not clean); determining if the data is corrupt (C 1, L 8-10; C 4, L 41-42; this is determined by the occurrence or non-occurrence of a cache failure of a first cache during a cache flush operation); if the data is not corrupt [if no failure has occurred] and the first cache line is not clean then writing [flushing] the data to the first memory location (C 9, L 26-27); marking the cache line available [clearing the dirty bit] (when the cache lines are written are to the persistent memory, the lines are cleared in the cache); determining at least one duplicate dirty cache line of the first dirty cache line and marking each of the at least one duplicate dirty cache line as an invalid cache line (C 7, L 63-65; when the data contains invalid data the cache lines are marked invalid).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2, 13, 17-18 and 19-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Loechel (USPN: 5,895,485).

Regarding claims 2 and 13, Loechel discloses the limitations cited above, however, Loechel does not explicitly disclose a multi-way set-associative. Official notice is taken that multi-way set-associative caches are well known in the art for providing improved performance by providing increased hit rates. Hence, it would have been obvious to one of ordinary skill.

Regarding claim 17-18, Loechel discloses receiving an instruction to write back at least one cache line to a memory (flush operation); selecting a cache line of a plurality of cache lines to write back to memory (when a flush operation occurs, the system selects the dirty lines to write back to memory); determine if the cache line is a clean line (intrinsically the systems determines this by determining that the line is dirty and needs to be flushed which also indicates that the line is not clean); determine a corresponding memory location in the memory to write back to by examining a tag portion of the cache line (the tag portion includes part of the main memory address and thus when the system writes the data to main memory [C 9, L 26-27], the system determines the corresponding memory location); determine if the cache line has data that is not corrupt (C 1, L 8-10; C 4, L 41-42; this is determined by the occurrence or non-occurrence of a

cache failure of a first cache during a cache flush operation); if the data is not corrupt [if no failure has occurred], then marking the cache line available [the cache line is marked available after the data has been flushed to memory]; writing the data back to the memory (C 9, L 26-27); determining if the cache line was a dirty cache line and if the cache line was a dirty cache line, then determining at least one duplicate dirty cache line if the first dirty cache line and marking the at least one duplicate dirty cache line invalid (C 7, L 63-65; when the data contains invalid data the cache lines are marked invalid); and if the cache line was not a dirty cache line, then repeating the steps beginning with selecting a cache line until no more associated cache lines exists (when the flush operation occurs, all the cache lines are searched for dirty cache lines, and the dirty cache lines are written back to memory and then cleared). Loechel does not disclose selecting a plurality of cache lines in an associated set of a cache to write back to memory. Loechel does not explicitly disclose a set associative cache. However, set associative caches are well known in the art for providing improved performance by improving the cache hit rate. Hence, it would have been obvious to one of ordinary skill in the art to use a set associative cache in Loechel's system wherein a plurality of cache lines are selected from an associated set of the cache for the desirable purpose of improved performance. Additionally, all hardware systems include computer readable mediums [memory] storing instructions [code] to execute operations [such as the above functions] of the system.

Regarding claim 19, Loechel discloses the limitations cited above, however, Loechel does not explicitly disclose a multi-way set-associative. Official notice is taken that multi-way set-

associative caches are well known in the art for providing improved performance by providing increased hit rates. Hence, it would have been obvious to one of ordinary skill.

Regarding claims 20-21, Loechel discloses an apparatus comprising a cache controller to intercept a request to write data to a cached memory location (C 6, L 52-56); determine associated cache lines corresponding to the memory location and write the data to a plurality of cache lines in the associated set that are available (C 6, L 52-59); and invoking a replacement policy to free cache lines in the associated cache if there are no cache lines available (Figure 8b, Reference 806; C 8, L 35-36). Loechel does not disclose a set associative cache. However, set associative caches are well known in the art for providing improved performance by improving the cache hit rate. Hence, it would have been obvious to one of ordinary skill in the art to use a set associative cache in Loechel's system wherein a plurality of cache lines are selected from an associated set of the cache for the desirable purpose of improved performance.

Regarding claims 22-24, Loechel discloses a main memory having at least one memory location that is cached to cache (Figure 2, Reference 208); a cache having a plurality of cache lines to store data (Figure 2, Reference 228); and a processor to receive an instruction to write data to a cached memory location (processing element within Reference 206 in Figure 2 which controls References 222-224); a cache controller to determine an associated cache line corresponding to the memory location, the associated line having a plurality of cache lines and to write the data to a plurality of available cache lines (Figure 2, Reference 226; C 6, L 52-59); and invoking a replacement policy to free cache lines in the associated cache if there are no cache lines available

(Figure 8b, Reference 806; C 8, L 35-36). Loechel does not disclose a set associative cache. However, set associative caches are well known in the art for providing improved performance by improving the cache hit rate. Hence, it would have been obvious to one of ordinary skill in the art to use a set associative cache in Loechel's system wherein a plurality of cache lines are selected from an associated set of the cache for the desirable purpose of improved performance.

Allowable Subject Matter

7. Claims 6-7, 9-11 and 15-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 703-308-9592. The examiner can normally be reached on M (10:00 - 6:30); Tues, Thr (10:00 - 4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 703-308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kimberly N. McLean-Mayo
Examiner
Art Unit 2187

KIMBERLY MCLEAN-MAYO
PRIMARY EXAMINER

KNM

June 21, 2004